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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/276,803	03/26/1999	BYOUNG-TAEK LEE	SEC.506	2646

7590 09/13/2002

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EXAMINER
BEREZNY, NEAL

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/276,803	LEE ET AL.	
	Examiner	Art Unit	
	Neal Berezny	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-8, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Al-Shareef et al. (6,162,744) in view of Ping et al. (5,882,979). Al-Shareef teaches forming a storage electrode, a high dielectric layer, a plate electrode, a first anneal at a first temp. at 600-800^{0}C, see claim 28, a second anneal at a second temp. less than the first temp. and at 100-600^{0}C, see claim 2, the high dielectric consisting of STO, BST, and PZT dielectrics, col.4, ln.5-6, the electrodes consisting of RuO_2 conductors, col.3, ln.55-60, forming an interdielectric over the capacitor, col.5, ln.29-30, and where the first and second anneals are performed after the formation of the high dielectric, col.4, ln.63-64. Al-Shareef appears not to specifically state that the two anneals be conducted in-situ. Ping teaches performing various processes in-situ, col.3, ln.4-5, fig.1 and 2, including an anneal step. It would be obvious to one of ordinary skill in the art at the time of the invention to combine Ping with Al-Shareef to perform the two anneal process steps in-situ in order to reduce the risk of contamination from the external environment. Further, official notice is given that it is well known and commonly practiced to employ clustering tools and in-situ processing to reduce processing time and exposure to the external environment, especially when the processing steps are very similar, requiring minimal variations between steps.

3. Al-Shareef, col.6, ln.13-15, col.5, ln.45-58, also teaches at least one of the two anneals to be conducted in a plasma environment, and under various environments, col.4, ln.17-39, but appears to be silent in specifying the specific equipment to be used to achieve these conditions. Official notice is given that given the teachings of Al-Shareef, it would be obvious to achieve the taught anneal conditions in well-known equipment commonly used for such applications, such as a furnace or in a vacuum RTP, and as suggested and anticipated by Al-Shareef they can be performed either separately or in-situ. One of ordinary skill in the art would be motivated to use commonly available equipment to achieve the taught anneals in order to keep process costs low.

4. Al-Shareef also teaches at least two multiple temperatures in multiple annealing steps, suggesting and anticipating more than two anneals. Al-Shareef appears not to specifically require that the third temp. be less than the second temp. It would be obvious to one of ordinary skill in the art to perform a third anneal at a lower temperature in order to reduce oxygen vacancy and densify the film, col.4, ln.55-57. Further, it has been held that a mere duplication of a process step, or the division of a single step into multiple steps, involves only routine skill in the art. *St. Regis Paper Co.* v. *Bemis Co.*, 193 USPQ 8. In addition, neither the claims nor the specifications disclose the critical nature nor unexpected results arising from a third anneal.

5. Claims 9-10, 12-13, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Al-Shareef et al. (6,162,744) in view of Azuma et al. (WO 96/02067 PCT) and Wolf, Vol.1, p.57. Al-Shareef teaches forming a storage electrode, a high dielectric layer, a plate electrode, a first anneal at a first temp. at 600-800^{0}C, see claim 28, a second anneal at a second temp. less than the first temp. and at 100-600^{0}C, see claim 2, the high dielectric consisting of STO, BST,

and PZT dielectrics, col.4, ln.5-6, the electrodes consisting of RuO_2 conductors, col.3, ln.55-60, forming an interdielectric over the capacitor, col.5, ln.29-30, and where the first and second anneals are performed after the formation of the high dielectric, col.4, ln.58-64.

6. Al-Shareef, col.6, ln.13-15, col.5, ln.45-58, also teaches at least one of the two anneals to be conducted in a plasma environment, and under various environments, col.4, ln.17-39, but appears to be silent in specifying the specific equipment to be used to achieve these conditions. Official notice is given that given the teachings of Al-Shareef, it would be obvious to achieve the taught anneal conditions in well-known equipment commonly used for such applications, such as a furnace or in a vacuum RTP, and as suggested and anticipated by Al-Shareef they can be performed either separately or in-situ. One of ordinary skill in the art would be motivated to use commonly available equipment to achieve the taught anneals in order to keep process costs low.

7. Al-Shareef also teaches at least two multiple temperatures in multiple annealing steps, suggesting and anticipating more than two anneals. Al-Shareef appears not to specifically require that the third temp. be less than the second temp. It would be obvious to one of ordinary skill in the art to perform a third anneal at a lower temperature in order to reduce oxygen vacancy and densify the film, col.4, ln.55-57. Further, it has been held that a mere duplication of a process step, or the division of a single step into multiple steps, involves only routine skill in the art. *St. Regis Paper Co.* v. *Bemis Co.*, 193 USPQ 8. In addition, neither the claims nor the specifications disclose the critical nature nor unexpected results arising from a third anneal.

8. Al-Shareef, while teaching the preferred embodiment, also anticipates performing one or both anneals after the formation of the second electrode, col.5, ln.6-10, but fails to elaborate on the specific combinations of anneals that should not be performed post plate electrode formation.

Azuma teaches performing the second anneal after the formation of the plate electrode, fig.4, el.P47, P48, and P50. Wolf teaches performing various interconnect thermal processes, which in terms of structure and function are also anneals, after the formation of the interdielectric, p.57, table 4, section 3. It would be obvious to one of ordinary skill in the art to combine the teachings of Azuma and Wolf to the anticipated processes of Al-Shareef, i.e. to perform thermal anneals after forming the plate electrode, to further include anneals, i.e. thermal interconnect processes, which would need to, or likely, be performed after either the formation of the plate electrode or after the formation of the interdielectric. It would be obvious to one of ordinary skill in the art to anticipate the process of performing one or both of the anneals, i.e. thermal interconnect processes, after either the formation of the plate electrode or the interdielectric, to complete the device and provide flat, low resistance interconnects. One would be motivated to combine Azuma and Wolf with Al-Shareef in order to reduce the post capacitor thermal budget and reduce the risk of oxidation of either of the electrodes from any out-diffusion of oxygen from the high dielectric layer, thereby reducing the capacitance of the capacitor. Official notice is given that it is well known in the art that various essential thermal interconnect processes, or anneals, are commonly performed throughout the industry, after the formation of the capacitor plate and the interdielectric layer. Further, such thermal processes, even when desired to be eliminated, cannot in practice be eliminated, because the consequences, for example non-planarized topography or non-silicided interconnects would result in poorly functioning devices and severe processing problems in subsequent steps. In conclusion, it is an almost an unavoidable requirement of devices to undergo several anneals after the formation of the capacitor.

Response to Arguments

9. Applicant's arguments filed 8/10/01 have been fully considered but they are not persuasive. Applicant's arguments with respect to claims 1-5, 7, 8, 11, and 14 involve a discussion of applicant's invention, but none of the claims contain all of the critical limitations and/or aspects that applicant alleges. Applicant is reminded that the examiner is required to interpret the claims as broadly as possible to identify infringement. Specifically, most of the claims do not require contain the limitation that the plate electrode consists of a metal oxide conductor, not a catalytic noble metal. Similarly, most of the claims do not contain the limitations regarding an oxygen atmosphere. Applicant's discussion of claim 1 is like-wise including many limitations simply not found in claim 1, such as a "reductive inert atmosphere", an oxygen atmosphere, and 4 hour anneals. Applicant argues that applicant's two step in-situ anneal is not obvious over the prior art of record because Ping uses in-situ processing for a variety of processes, including annealing, col..3, ln.7, 38-41, but not for two annealing steps. If a skilled artisan, using Ping, could anticipate combining two dissimilar processes, such as an implant and an anneal step, or a CVD process with an anneal, into the same piece of equipment, in order to reduce surface contamination and improve process efficiency, then clearly combining two very similar processes, such as two anneals, into the same equipment would be very obvious and very easy to implement, relative to combining two dissimilar processes.

10. Applicant traverses examiner's 103 rejection of claims 9, 10, 12, 13, and 15-20 on the grounds that applicant's claimed invention requires that the two anneals be performed after the formation of the plate electrode. Applicant provides a discussion as to the merits of performing the second anneal at a temperature lower than the first anneal. The issue appears not to be

related to a temperature difference issue, but rather, to a post-plate electrode issue, so applicant's meaning is unclear.

11. Applicant also argues that catalytic noble metals are easily oxidized and the Al-Shareef reference seeks to avoid oxidizing the plate electrode from the dielectric. None of the claims at issue, contain all the limitation presented in applicant's arguments, specifically, that the plate electrode is composed of a noble metal and the second anneal is performed in an oxygen atmosphere to remove oxygen vacancies. Regarding applicant's arguments related to Al-Shareef, applicant's attention is directed to the **entire** passage cited by examiner, col.5, ln.6-10, specifically col.5, ln.7-10. Al-Shareef discusses a preferred embodiment, wherein it is specifically stated that it is not desirable to perform the anneals after the formation of the plate electrode and then proceeds to explain why. Clearly, Al-Shareef anticipated performing the anneals after the formation of the plate electrode, but concluded that such a strategy was undesirable for the reasons disclosed by the reference, and therefore, elected to perform the anneals before the formation of the plate electrode. The reference need not agree with applicant to have anticipated the claimed invention.

12. Further, Wolf teaches the effects of thermal processing and the use of thermal budgets, which is well known in the art. The table and section cited are a listing of thermal processes performed when forming interconnects. Since interconnects are formed after the formation of capacitors and all thermal processes anneal the structure, then one of ordinary skill in the art would realize that a number of anneals are commonly performed after the formation of the capacitor. Therefore, Wolf teaches that anneals, or thermal processes, occur after the formation of the capacitor and the interdielectric layer. Applicant is reminded that the examiner must

interpret the claims as broadly as possible and that the examiner can have different reasons for combining the references, than the applicant.

CONCLUSION

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neal Berezny whose telephone number is (703) 305-1481. The examiner can normally be reached on Monday to Friday from 9:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached at (703) 308-4918. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

Neal Berezny
9/7/02

Neal Berezny

Patent Examiner

Art Unit 2823